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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,246	04/01/2004	Takahiro Okuno	251363US2	6970

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,246	OKUNO ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-14 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 01 April 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because they do not include a cross-sectional view of the semiconductor devices according to claims 5 and 13, "wherein the second emitter layer is formed as island shaped patterns each having opposite ends in contact with the trenches opposed to each other via the base layer in each dummy cell region". In order to gain a better understanding of applicant's invention, applicant is requested to file new drawings showing a cross-section including the second emitter corresponding to plan layouts in Figs. 7 and 9. The drawings are also objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Fig. 10 does not include reference 62 mentioned on page 14, line 14 of the specification. Perhaps reference 12 in Fig. 10 was meant to be 62. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

1. The abstract of the disclosure is objected to because it: fails to disclose the improvement made; contains extensive design details; and exceeds 150 words.

Correction is required. See MPEP § 608.01(b).

2. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The disclosure is objected to because of the following informalities: the reference "No. 10,354,048" on page 12, line 17 should appear "No. 10/354,048"; reference 62 on page 14, line 14 does not appear in fig 10 (should 12 be 62?); also page 14, line 14 refers to "IEGT 6 shown in Fig. 11", IEGT 6 is shown in Fig. 10, not Fig. 11.

Appropriate correction is required.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Injection enhanced gate transistor including second emitter in dummy cell region to avoid waveform oscillation associated with negative gate capacitance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4,6, and 8-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka (US Pub. No. 2003/0042525), hereinafter Tanaka.

8. A copy of Fig. 13 from Tanaka is provided with additional references to clarify comparisons made by the examiner. The figure is identical to the original figure from

Tanaka, with the exception that six new reference labels have been added. The added reference labels have been given letter designations to distinguish them from the original numbered reference labels.

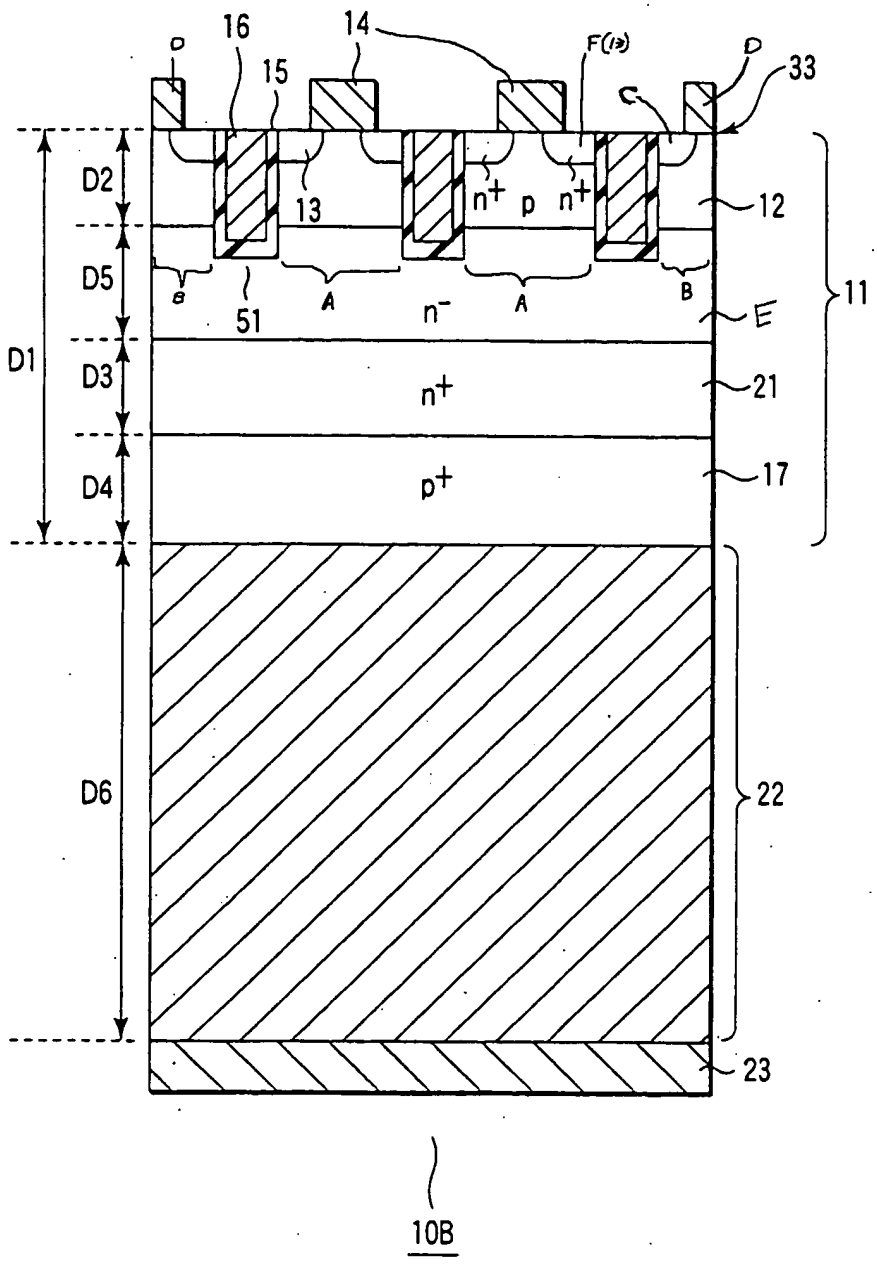

FIG. 13

9. Regarding claims 1 and 8, Tanaka discloses a semiconductor device comprising:

a drift layer (E) of a first conductivity type;

a collector layer (17) of a second conductivity type located on the drift layer;

a collector electrode (22,23) located on the collector layer;

a base layer (12) of the second conductivity type located in a region isolated from the collector layer on the drift layer;

a plurality of trenches (51) formed at certain intervals to extend from the top surface of the base layer into the drift layer and thereby divide the base layer to main cell regions (A) and dummy cell regions (B);

a first emitter layer (13) of the first conductivity type selectively formed in the surface layer of the base layer in each main cell region to extend along adjacent one of the trenches;

gate electrodes (16) formed in the trenches sandwiching each main cell region among said plurality of trenches via a gate insulating film (15);

an emitter electrode (14) located over the base layer and the first emitter layer in each main cell region; and

a second emitter layer (C) of the first conductivity type selectively formed so as to be scattered in the surface layer of the base layer in each dummy region and having a surface area smaller than that of the first emitter layer. Note that Fig. 13 clearly shows second emitter layer (C) smaller than first emitter 13. With respect to this comparison, drawings may not be interpreted as providing exact dimensions, but may be interpreted to indicate relative sizes.

10. Further regarding claim 8, Tanaka inherently discloses "wherein resistance value of a floating resistor as a resistance between the base layer or the dummy cell region and the emitter electrode is adjusted to be smaller than the resistance value causing rise of the gate-emitter voltage due to negative capacitance of the gate in a period to charge a gate charge between the gate and the collector by a voltage applied between the gate and the emitter when the device is turned on." Since Tanaka discloses the same structure as the applicant's, it functions similarly.

11. Regarding claims 2 and 9, it is known to one of ordinary skill in the art that the impurity implantation process by nature provides an impurity concentration profile having a peak on the implantation side, the side of the first emitter.

12. Regarding claims 3 and 10, Tanaka discloses the semiconductor device set forth in the claims, therefore his device is capable of functioning in the same manner "wherein the drift layer of the main cell region forms a current path narrow enough to accumulate a carrier of the second conductivity type on and around the bottom of the trenches when the device is turned on, and wherein the second emitter layer forms a current path conducting a carrier of the second conductivity type to the emitter electrode by an amount no affecting the injection efficiency of the carrier of the first conductivity type from the emitter electrode to the drift layer when the device is turned on."

13. Regarding claims 4 and 12, it is known to one of ordinary skill in the art that the manufacture of semiconductor devices such as Tanaka's and the applicant's frequently results in a layout in which cross-sections like Tanaka's Fig. 13 or applicant's Fig. 2 are repeated in a lateral direction (for example, applicants Fig. 1). Therefore, each dummy

cell region (B) will have trenches on either side "wherein the second emitter layer is formed as isolated patterns in contact with the trenches opposed to each other via the base layer in each dummy cell region."

14. Regarding claims 6 and 11, Tanaka further discloses "a via contact (D) formed in contact with the second emitter layer (C) to connect the base layer (12) in the dummy cell region (B) to the emitter electrode (14) via the second emitter layer,"

Additionally, Tanaka discloses "wherein the resistance value of a floating resistor as a resistor between the base layer of the dummy cell region and the emitter electrode is adjusted by geometries of the second emitter layer and the via contact", due to the mere presence of the claimed structure.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 5, 7, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka.

17. Regarding claims 5 and 13, Tanaka discloses the semiconductor devices having the second emitter layer (D) formed as patterns in contact with the trenches (51) opposed to each other via the base layer in each dummy cell region.

18. Tanaka does not disclose "the second emitter layer is formed as island shaped patterns each having opposite ends in contact with the trenches."

19. However, such difference is regarded as nothing more than an obvious variation of Tanaka. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to connect the isolated second emitter regions opposing one another in each dummy cell region to one another, forming a continuous island-pattern second emitter region with opposite ends in contact with the trenches opposed to each other.

20. The ordinary artisan would have been motivated to modify Tanaka in the manner described above for at least the purpose of enhanced electrical effect of second emitter region, enlarging the second emitter region.

21. Regarding claims 7 and 14, Tanaka does not disclose "the resistance value of the floating resistor is 0.3Ω – 3Ω when the applied voltage between the collector and the emitter is 600V and the gate resistance is 51Ω".

22. However, such difference is regarded as nothing more than an obvious design choice. That is, varying parameters such as size, concentration, and resistivity merely requires routine experimentation. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to adjust the resistance value of the floating resistor to between 0.3Ω – 3Ω when the applied voltage between the collector and the emitter is 600V and the gate resistance is 51Ω.

23. The ordinary artisan would have been motivated to modify Tanaka in the manner described above for at least the purpose of device stability.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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